PATENT
ATTORNEY DOCKET NO. 72291

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Bradford L. Farris James J. Fitzgibbon
Appln. No.	
Filed:	Herewith
Title:	ROLLING CODE SECURITY SYSTEM
Group Art Unit:	
Examiner:	

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number

EL 868370920 US

Date of Deposit October 17, 2001

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Edward Price
(Typed or printed name of person mailing)

Edward Price
(Signature of person mailing)

Hon. Commissioner of Patents and Trademarks
Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

This Amendment is being filed along with the above-captioned application. Upon establishing a filing date for the above-captioned application, please enter the following amendments:

IN THE CLAIMS:

Please add the following new claims 17 through 41:

17. A transmitter for sending an encrypted signal to control an actuator, comprising:

oscillator for generating a radio frequency oscillatory signal;

apparatus for enabling the sending of an encrypted signal;

binary code generator responsive to the enabling apparatus for generating a variable binary code, said variable code being different for each enabling by the enabling device;

multi-value digit code generator for generating a multi-value digit code responsive to the variable binary code, wherein each multi-value digit has at least three possible values; and

transmitting apparatus for modulating the radio frequency oscillatory signal with the multi-value digit code to produce a modulated multi-value digit coded variable radio frequency signal for operation or control of a secure actuator.

18. A transmitter for sending an encrypted signal to control an actuator according to claim 17, further comprising apparatus for receiving said variable binary signal and producing a mirrored binary signal, said mirrored binary signal being supplied to said multi-value digit code generator for generating the multi-value digit signal from the variable binary signal.

19. A transmitter for sending an encrypted signal to control an actuator according to claim 17, comprising apparatus for producing a fixed code signal and for combining said fixed code signal with a rolling code signal.

20. A transmitter for sending an encrypted signal to control an actuator according to claim 19, comprising apparatus for interleaving multi-value digits derived from said fixed code signal with multi-value digits derived from

said rolling code signal to produce a multi-value digit interleaved fixed and rolling code signal.

21. A transmitter for sending an encrypted signal to control an actuator according to claim 17, comprising incrementing apparatus for altering said variable code by adding a fixed value with each enabling apparatus actuation.

22. A transmitter for sending an encrypted signal to control an actuator according to claim 21, wherein said means for incrementing said variable code increments said variable code by a prime number value.

23. A transmitter for sending an encrypted signal to control an actuator according to claim 17, wherein said binary code generator for generating a variable binary code includes a non-volatile memory for storing a variable binary code.

24. A transmitter for sending an encrypted signal to control an actuator according to claim 17, wherein said binary code generator for generating said variable code includes storage means holding a previous cycle variable code signal from which the variable code is generated.

25. A remote security system for communicating an encrypted signal to a control actuator, comprising:

binary code generator for generating a sequence of variable binary codes according to a predetermined algorithm, successive codes in the sequence being different from preceding codes in the sequence;

multi-value digit code generator for converting said generated variable binary code to a multi-value digit code, wherein each multi-value digit has at least three possible values;

a transmitter for modulating a transmitted radio frequency signal with said multi-value digit code;

a radio-frequency receiver for demodulating said transmitted modulated radio frequency signal and providing a received multi-value digit code;

multi-value digit code convertor for converting said received multi-value digit code to a received binary code;

a controller responsive to a positive comparison of said received binary code and a reference variable binary code; and

update apparatus responsive to said positive comparison for updating said reference variable binary code according to said received binary code.

26. A remote security system according to claim 25, wherein said update apparatus updates said reference variable binary code by performing said predetermined algorithm on said reference variable binary code.

27. A remote security system according to claim 25, wherein said positive comparison results if said received binary code and said reference variable binary code lie within a predetermined numerical limit of one another.

28. A remote security system according to claim 27, wherein said positive comparison results if the numerical difference of said received binary code minus said reference

variable binary code is a positive number less than said predetermined limit.

29. A remote security system according to claim 28, wherein said predetermined limit is about 1000.

30. A remote security system according to claim 28, wherein said positive comparison results if at least two said received binary codes transmitted in succession, each of which is numerically different from said reference variable binary code by a number outside the range of said predetermined limit, represent successive results of said predetermined algorithm.

31. A remote security system according to claim 30, wherein said positive comparison results if said successively transmitted codes which represent successive results of said preselected algorithm, each yield a difference when subtracted from said reference variable binary code outside the range of zero to a second predetermined limit.

32. A remote security system according to claim 31, wherein said second predetermined limit is about 300.

33. A remote security system according to claim 27, wherein the variable binary code is a rolling code and the system further comprises a binary code combiner for combining a binary fixed code with said binary rolling code and providing the combination to said multi-value digit code generator.

34. A remote security system according to claim 33, further comprising apparatus for interleaving multi-value digits derived from said binary fixed code with multi-value digits derived from said binary rolling code to provide an interleaved multi-value digit fixed-and-rolling code to said transmitter.

35. A remote security system according to claim 34, further comprising apparatus for receiving said output of said radio-frequency receiver and separating said interleaved fixed-and-rolling code and providing to said multi-value digit code convertor a received multi-value digit fixed code and a received multi-value digit rolling code.

36. A remote security system according to claim 35, wherein said multi-value digit code convertor provides a received binary fixed code in response to said received multi-value digit fixed code and a received binary rolling code in response to said received multi-value digit rolling code, and further comprising addressing apparatus for using said received binary fixed code to address said reference variable binary code in a memory.

37. A remote security system according to claim 36, further comprising means for mirroring said binary rolling code and providing it to said multi-value digit code generator.

38. A remote security system according to claim 37, further comprising apparatus for mirroring said received binary rolling code and providing it to said controller and to said update apparatus.

39. A remote security system according to claim 38, wherein said predetermined algorithm generates a variable binary code by adding a numeric constant to it.

40. A remote security system according to claim 39, wherein said predetermined algorithm generates a variable binary code by adding the value 3 to it.

41. A remote security system according to claim 31, further comprising second update apparatus for updating said reference variable binary code according to one of the set of said successively transmitted received binary codes.

Please cancel claims 1 through 16.

REMARKS

Upon entry of the instant amendment, claims 17-41 are pending in the instant application. The claims of the instant application refer generally to multi-valued digits. As set forth in the claims, each multi-value digit has at least three possible values.

Applicants respectfully request entry of the amendments set forth hereinabove, and submit that no new matter has been added.

The Commissioner is hereby authorized to charge any additional fees which may be required with respect to this communication or credit any overpayment to Deposit Account No. 06-1135.

Respectfully submitted,
FITCH, EVEN, TABIN & FLANNERY

Dated: October 17, 2001

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Edward Price

(Typed or printed name of person mailing)

Edward Price

(Signature of person mailing)

SUBMISSION OF FORMAL DRAWINGS

Director-U.S. Patent and Trademark Office
Attn. Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed herewith are sixteen (16) sheets of formal drawings (FIG. 1 through FIG. 8F). FIG. 5 as originally filed has been divided into FIGS. 5A-B. This and other minor drawing changes are discussed in the accompanying Request for Examiner Approval of Drawing Corrections. Please substitute these formal drawings for the informal drawings submitted with the filing of the above-captioned application.

Respectfully submitted,
FITCH, EVEN, TABIN & FLANNERY

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(Signature of person mailing)

REQUEST FOR EXAMINER APPROVAL OF DRAWING CORRECTION

Director-U.S. Patent and Trademark Office
Attn. Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed herewith are fifteen (15) sheets of drawings (FIG. 1 through FIG. 8F) for the above-captioned application, showing corrections to be made in RED permanent ink.

Sheets 1-3 contain no drawing changes.

Fig. 4 has been amended to remove the notation identifying the individual logic component values and unused reference numerals.

To comply with formal drafting requirements, FIG. 5 has been divided into FIGS. 5A-B.

FIGS. 5A and 5B have been amended to remove the notation identifying the individual logic component values and unused reference numerals.

FIG. 6 has been amended to eliminate unnecessary language.

FIGS. 7-8F have been amended to eliminate the additional set of reference numerals listed in the flow charts.

Lastly, FIG. 7C has been amended to clarify the transfer of control from step 534. Specifically, the branch extending from step 534 to 536 has been amended to indicate that this transfer occurs if an ODD bit count is detected. Likewise, the branch extending from step 534 to 538 has been amended to indicate that this transfer occurs if an EVEN bit count is detected. Support for this change can be found on page 13, lines 22-27 of the specification.

The Applicants submit that no new matter has been added and respectfully request Examiner approval of the enclosed drawing corrections.

Respectfully submitted,
FITCH, EVEN, TABIN & FLANNERY

Date: October 17, 2001

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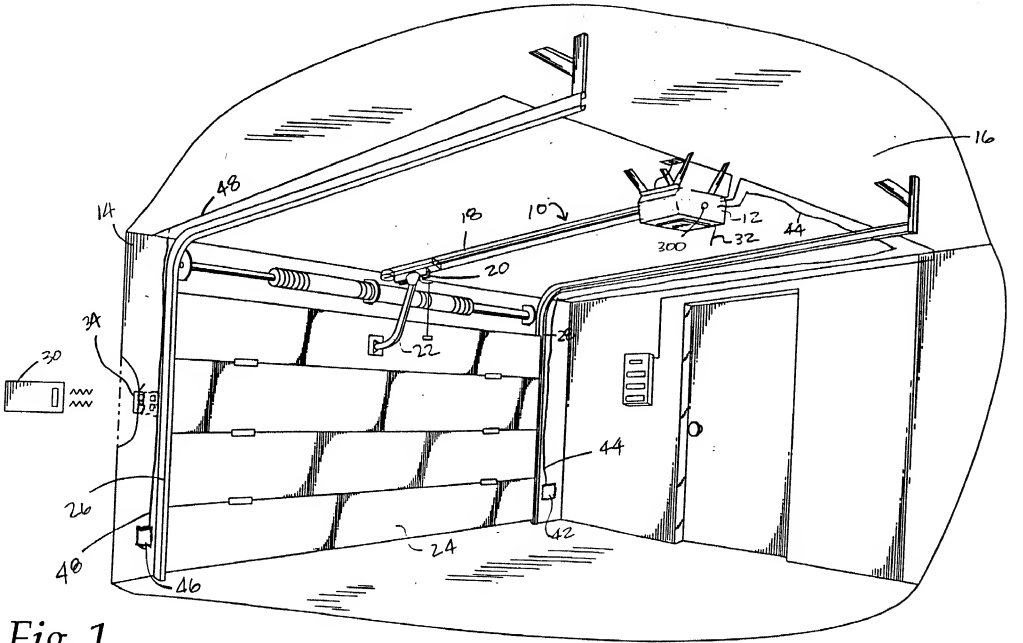
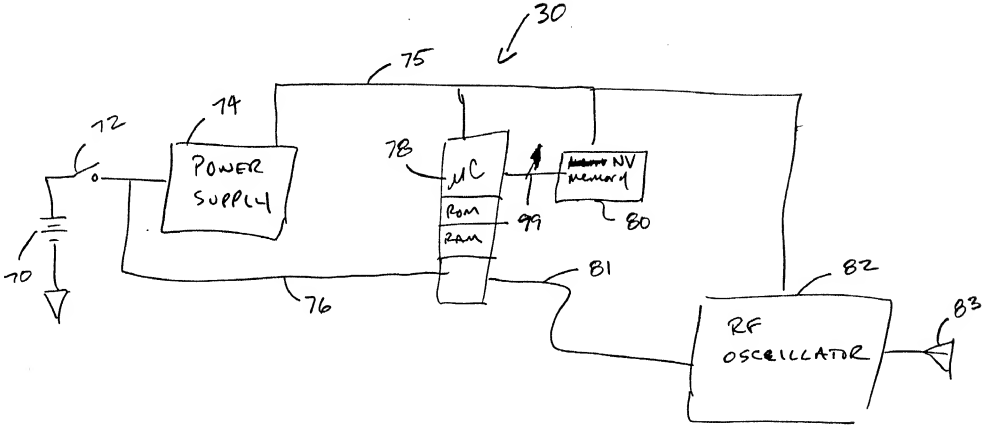


Fig. 1


30
75
74
72
78
μC
NV memory
POWER SUPPLY
ROM
RAM
99
80
70
76
81
82
RF OSCILLATOR
83

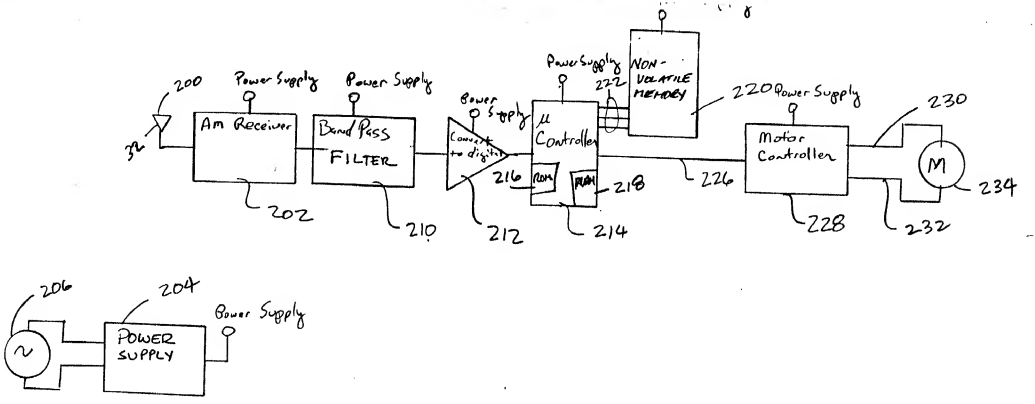

200
Power Supply
Power Supply
Power Supply
Power Supply
272
NON-VOLATILE MEMORY
220
Power Supply
230
AM Receiver
Band Pass FILTER
Converter to digital
μ Controller
ROM
RAM
216
218
226
Motor Controller
M
234
202
210
212
214
228
232
206
204
Power Supply
POWER SUPPLY

FIG 3

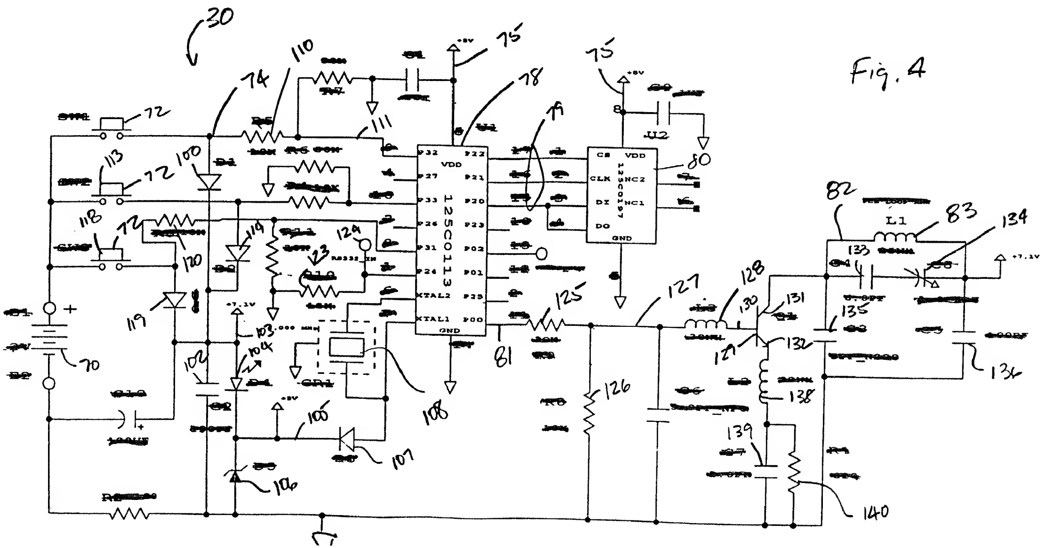

125C0113
VDD
P32
P27
P33
P26
P31
P24
XTAL2
XTAL1
GND
P22
P21
P20
P23
P02
P01
P25
P00
125C0197
CS
CLK
DI
DO
NC2
NC1
+5V
+7.1V
RS232_IN
L1

Fig. 4

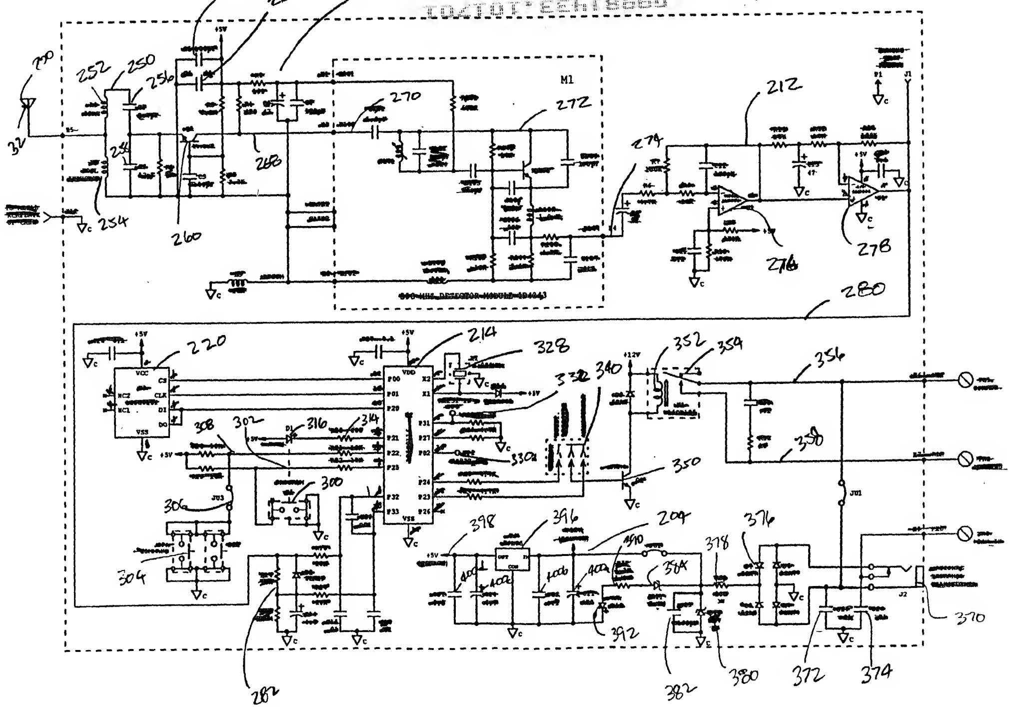
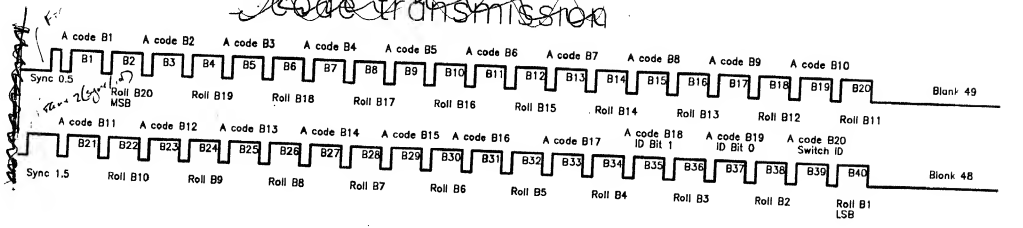
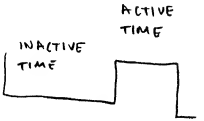

M1
+5V
+12V
VCC
CS
CLK
DI
DO
VSS
NC1
NC2
VDD
X1
X2
P00
P01
P20
P21
P22
P23
P24
P23
P26
P31
P27
P02
P32
P33
VSS
J1
J2
JU1
JU3
D1
202
212
214
220
250
252
254
256
258
260
262
264
268
270
272
274
276
278
280
282
290
32
300
302
304
306
308
314
316
328
330a
332
340
350
352
354
356
358
370
372
374
376
378
380
382
384
390
392
396
398
400a
400b
204

Fig. 5

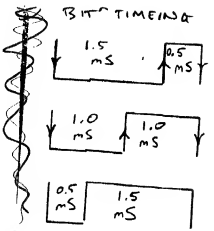
Code transmission





BIT VALUE

ACTIVE TIME - INACTIVE TIME



0.5 - 1.5 = -1.0 MILLISECONDS

1.0 - 1.0 = 0

1.5 - 0.5 = 1.0

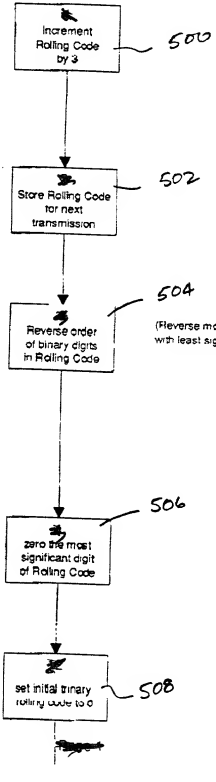


Fig. 7A

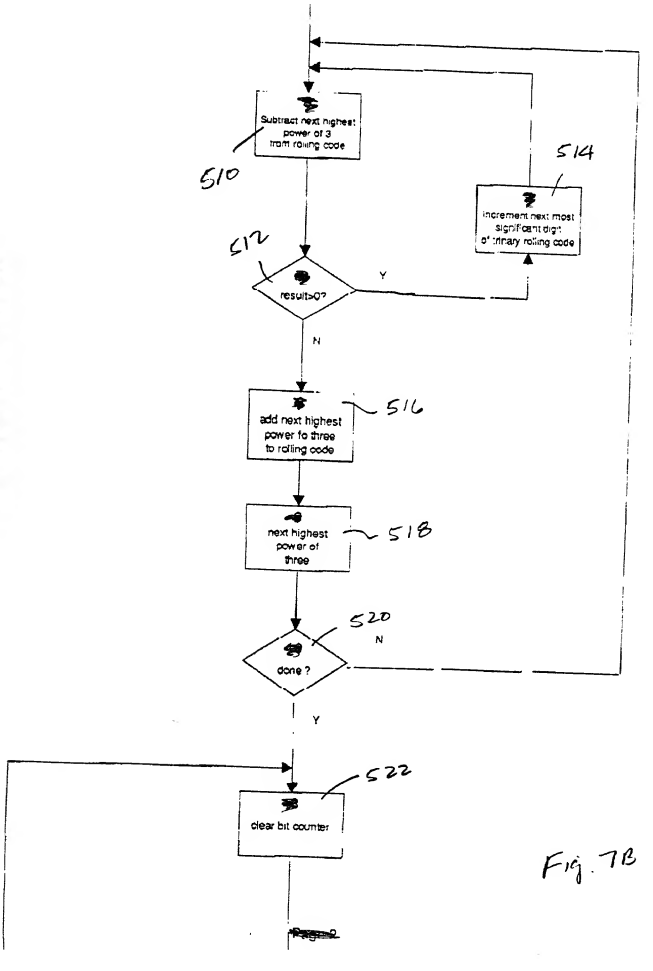

Subtract next highest power of 3 from rolling code
510
514
Increment next most significant digit of ternary rolling code
512
result>0?
Y
N
add next highest power to three to rolling code
516
next highest power of three
518
520
N
done ?
Y
522
clear bit counter

Fig. 7B

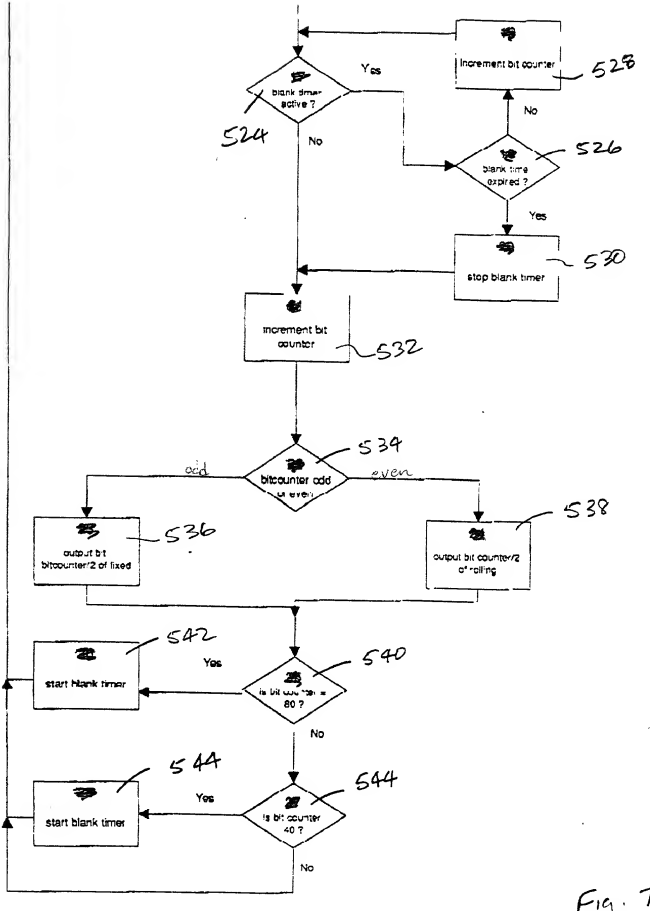

Increment bit counter
528
blank timer active ?
Yes
No
524
blank time expired ?
526
Yes
stop blank timer
530
increment bit counter
532
bitcounter odd or even
534
odd
even
output bit bitcounter/2 of fixed
536
output bit counter/2 of rolling
538
start blank timer
542
Yes
is bit counter = 80 ?
540
No
start blank timer
544
Yes
is bit counter 40 ?
544
No

Fig. 7C

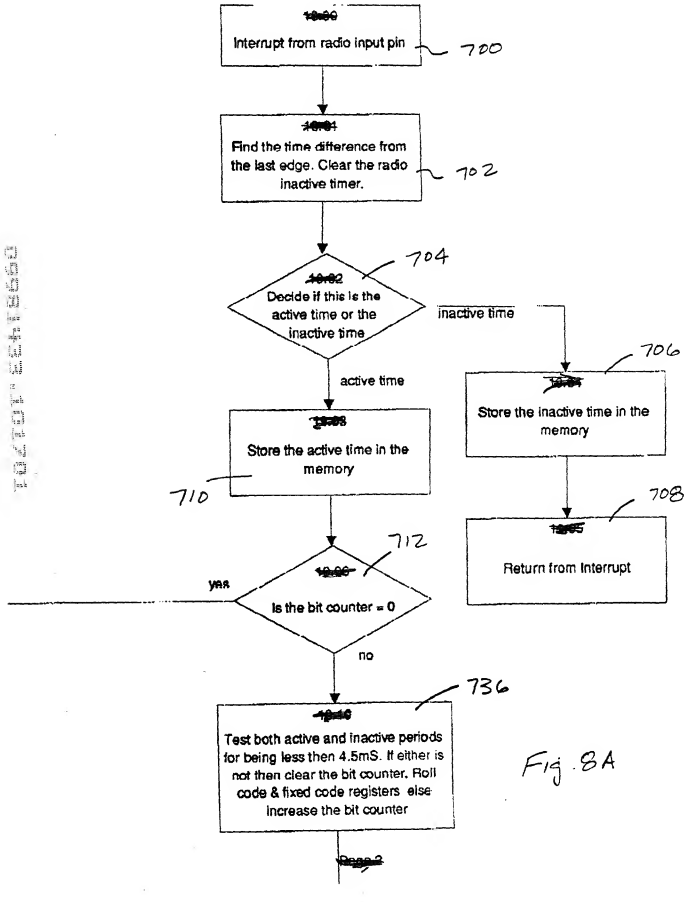

Interrupt from radio input pin
700
Find the time difference from the last edge. Clear the radio inactive timer.
702
Decide if this is the active time or the inactive time
704
inactive time
active time
Store the inactive time in the memory
706
Store the active time in the memory
710
Return from Interrupt
708
Is the bit counter = 0
712
yes
no
Test both active and inactive periods for being less then 4.5mS. If either is not then clear the bit counter. Roll code & fixed code registers else increase the bit counter
736
Page 2

Fig. 8A

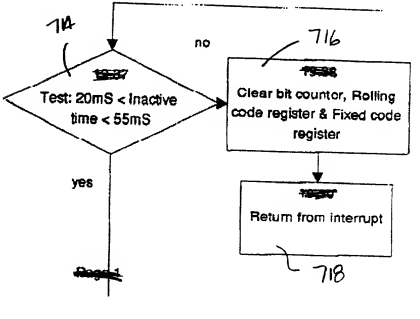

714
no
716
Test: 20mS < Inactive time < 55mS
Clear bit countor, Rolling code register & Fixed code register
yes
Return from interrupt
718

Fig. 8B

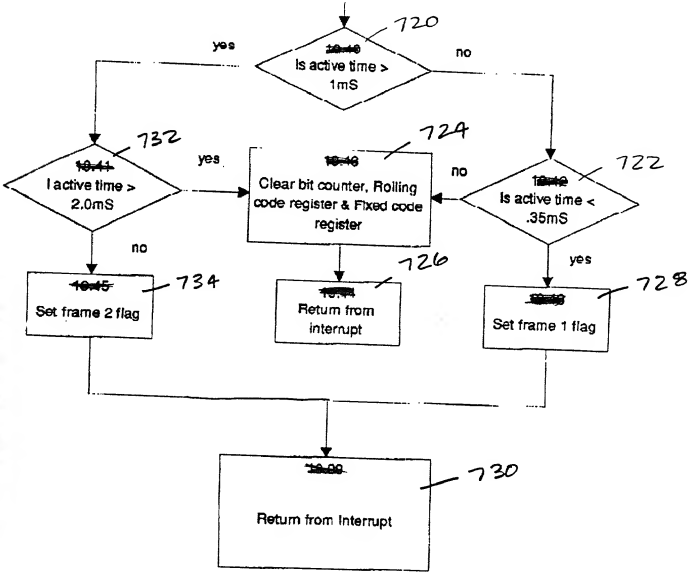

720
Is active time > 1mS
yes
no
732
Is active time > 2.0mS
yes
724
Clear bit counter, Rolling code register & Fixed code register
no
722
Is active time < .35mS
no
734
Set frame 2 flag
726
Return from interrupt
yes
728
Set frame 1 flag
730
Return from Interrupt

Fig. 8C

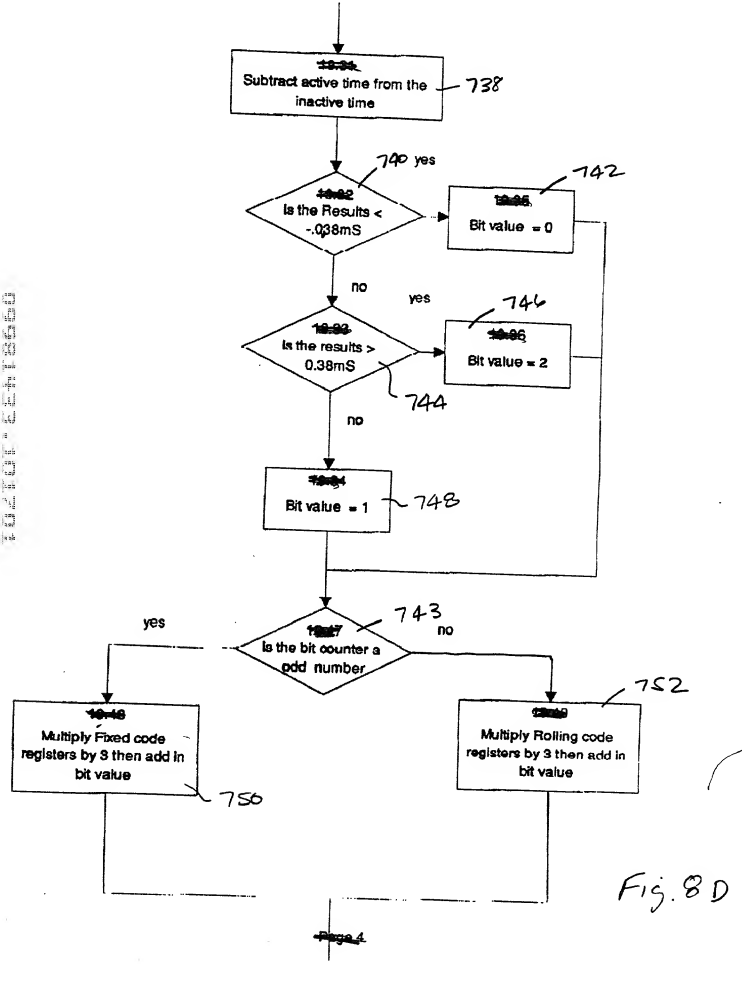

Subtract active time from the inactive time
738
740
yes
Is the Results < -.038mS
742
Bit value = 0
no
yes
746
Is the results > 0.38mS
Bit value = 2
744
no
Bit value = 1
748
yes
743
Is the bit counter a odd number
no
752
Multiply Fixed code registers by 3 then add in bit value
750
Multiply Rolling code registers by 3 then add in bit value
Page 4

Fig. 8D

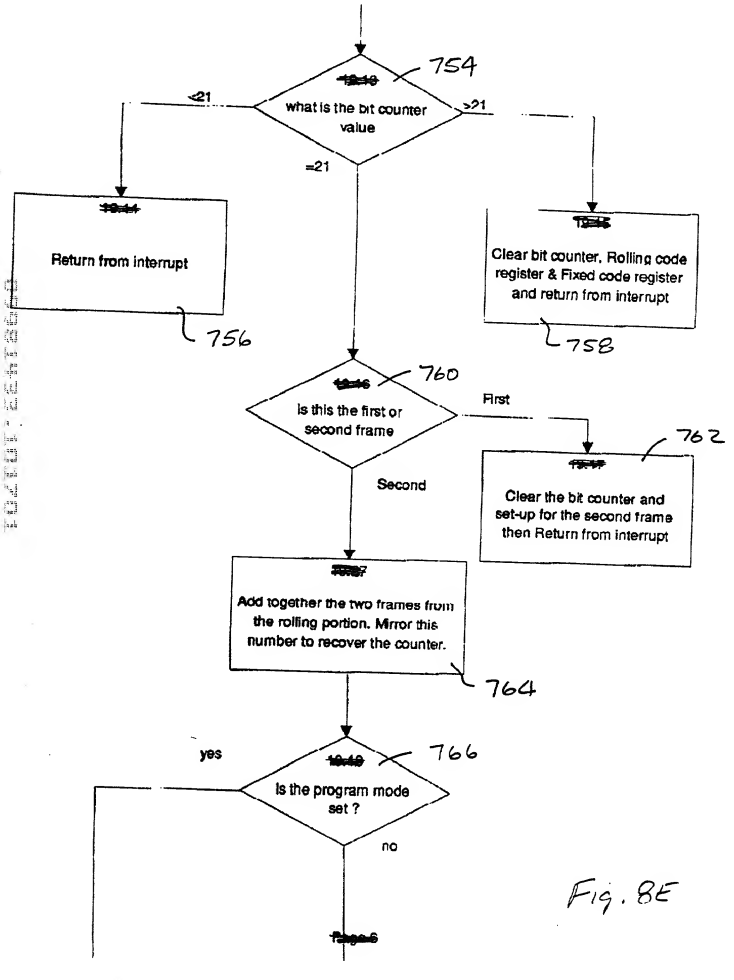

754
what is the bit counter value
<21
=21
>21
Return from interrupt
756
Clear bit counter, Rolling code register & Fixed code register and return from interrupt
758
760
Is this the first or second frame
First
Second
762
Clear the bit counter and set-up for the second frame then Return from interrupt
Add together the two frames from the rolling portion. Mirror this number to recover the counter.
764
yes
766
Is the program mode set ?
no

Fig. 8E

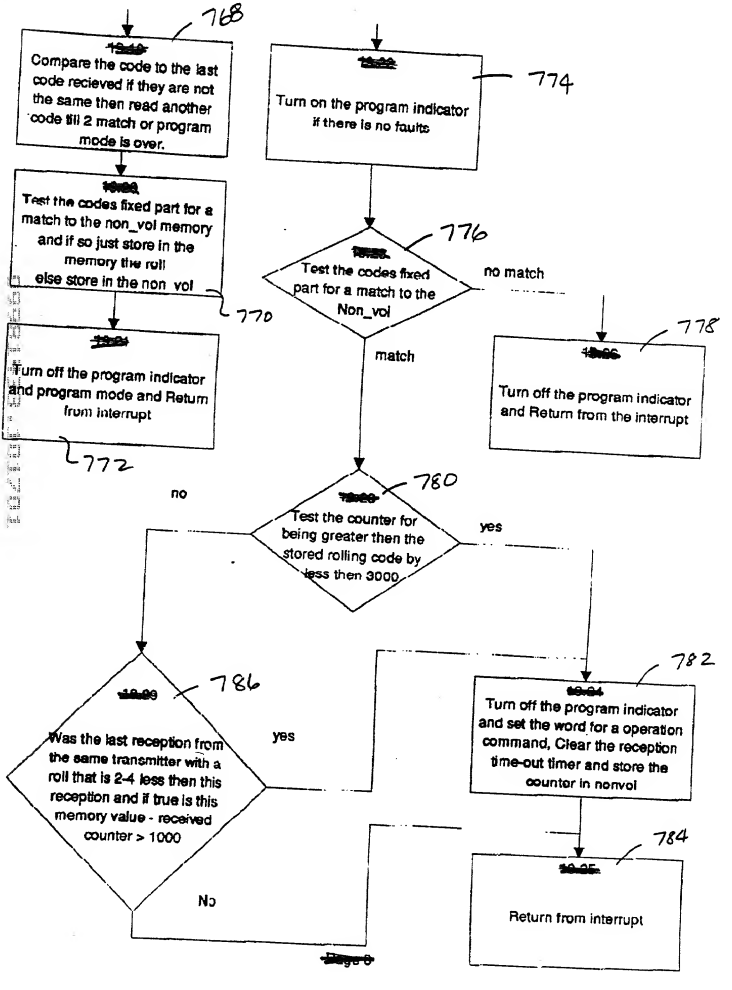

768
Compare the code to the last code recieved if they are not the same then read another code till 2 match or program mode is over.
774
Turn on the program indicator if there is no faults
Test the codes fixed part for a match to the non_vol memory and if so just store in the memory the roll else store in the non vol
776
Test the codes fixed part for a match to the Non_vol
no match
match
770
778
Turn off the program indicator and program mode and Return from interrupt
Turn off the program indicator and Return from the interrupt
772
no
780
Test the counter for being greater then the stored rolling code by less then 3000
yes
782
Turn off the program indicator and set the word for a operation command, Clear the reception time-out timer and store the counter in nonvol
786
Was the last reception from the same transmitter with a roll that is 2-4 less then this reception and if true is this memory value - received counter > 1000
yes
No
784
Return from interrupt

Fig. 8F